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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/628,184

07/28/2000

Frankie F. Roohparvar

400.007US01

2677

7590

04/07/2004

Fogg Slifer & Polglaze PA

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EXAMINER

PEIKARI, BEHZAD

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 04/07/2004

9

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/628,184

Applicant(s)

ROOHPARVAR, FRANKIE F.

Examiner

B. James Peikari

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2003 and 28 July 2000.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) 11 and 21-30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 12-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The previous rejections under 35 USC § 102 of the claims elected on January 15, 2004 are withdrawn due to the amendment filed on October 6, 2003.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-10 and 12-20 are rejected under 35 U.S.C. 103 as being unpatentable in view of Hazen et al., U.S. 6,088,264. The Microsoft Press Computer Dictionary, 2nd ed. is cited for definition purposes only to describe the state of the art at the time of the invention.

Applicant's disclosure and claims mention the use of banks in a non-volatile memory. The Microsoft Press Computer Dictionary, 2nd ed. defines a bank as "any

group of similar electrical devices connected together for use as a single device...In computer hardware, *bank* is used to refer to a section of memory, usually of a size convenient for a CPU to address". Furthermore, this dictionary defines block as "Literally, a group of similar things – usually bytes of storage or data."

The present invention includes an array of non-volatile memory cells arranged in a plurality of addressable banks. The read/write circuitry coupled to the array allows data to be simultaneously written to one bank while data is read from two or more remaining banks of the plurality of addressable banks. Thus, applicant's invention requires at least three non-volatile memory banks to operate as claimed.

Hazen et al. teach a synchronous non-volatile flash memory device divided into a number of partitions (note Figure 2 or 3) wherein each partition operates as a bank since each is implemented as a physically separate device on a different physical plane (column 2, lines 23-28) and each may be addressed independently of the others. The flexible design of the Hazen et al. system allows for any combination of the reading, writing, or erasing to occur to any number the partitions simultaneously. Thus, for a two partition system, e.g. partitions A and B, nine different combinations of read, write or erase transaction(s) may occur at any given time. Similarly, for a three partition system, e.g., partitions A, B and C, nineteen different combinations of read, write or erase transaction(s) may occur at any given time, including the claimed writing to a partition A while reading from partitions B and C.

As for including a write latch, four blocks, and multiple processors, these were all well known features used with non-volatile memories at the time of the invention. It

would have been obvious to one having ordinary skill in the art to include each of these in the system of Hazen et al. since (a) a write latch would have facilitated timing of data transfers, which is extremely necessary in synchronous systems such as that of Hazen et al., (b) four "blocks" was a very relative term in the art, and appears to have been well within the scope of the Hazen et al. system, which could flexibly divide the array into partitions having different numbers of blocks (note partition 305 vs partition 315), and (c) multiprocessors generally worked in parallel to provide faster processing, which would have been extremely useful in conjunction with the multiple, independently-addressable partitions of the Hazen et al. system for fast results.

5. Claims 1-10 and 12-20 are rejected under 35 U.S.C. 103 as being unpatentable in view of Nawaki, U.S. 6,081,450. The Microsoft Press Computer Dictionary, 2nd ed. is cited for definition purposes only to describe the state of the art at the time of the invention.

Applicant's disclosure and claims mention the use of banks in a non-volatile memory. The Microsoft Press Computer Dictionary, 2nd ed. defines a bank as "any group of similar electrical devices connected together for use as a single device...In computer hardware, *bank* is used to refer to a section of memory, usually of a size convenient for a CPU to address". Furthermore, this dictionary defines block as "Literally, a group of similar things – usually bytes of storage or data."

The present invention includes an array of non-volatile memory cells arranged in a plurality of addressable banks. The read/write circuitry coupled to the array allows

data to be simultaneously written to one bank while data is read from two or more remaining banks of the plurality of addressable banks. Thus, applicant's invention requires at least three non-volatile memory banks to operate as claimed.

Nawaki teaches a synchronous non-volatile flash memory device divided into a number of regions (note Figure 2) wherein each "block" or "region" operates as a bank since each region may be independently operated upon (column 8, lines 19-29) . The flexible design of the Nawaki system allows for any combination of the reading, writing, or erasing to occur to any number of regions simultaneously. Thus, for a two region system, e.g. regions 1 and 2, nine different combinations of read, write or erase transaction(s) may occur at any given time. Similarly, for a three region system, e.g., regions 1, 2 and 3, nineteen different combinations of read, write or erase transaction(s) may occur at any given time, including the claimed writing to a region 1 while reading from regions 2 and 3.

As for including a write latch, four blocks, and multiple processors, these were all well known features used with non-volatile memories at the time of the invention. It would have been obvious to one having ordinary skill in the art to include each of these in the system of Nawaki since (a) a write latch would have facilitated timing of data transfers, which is extremely necessary in synchronous systems such as that of Hazen et al., (b) four "blocks" was a very relative term in the art, and appears to have been well within the scope of the Nawaki system, which could flexibly divide the array into regions (also called "blocks", although not necessarily equivalent to applicant's "blocks") of different sizes and (c) multiprocessors generally worked in parallel to provide faster

processing, which would have been extremely useful in conjunction with the multiple, independently-addressable regions of the Nawaki system for fast results.

Double Patenting

6. The previous provisional obviousness-type double patenting rejection of the claims elected on January 15, 2004 is withdrawn due to the amendment filed on October 6, 2003.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824. The examiner is generally available between 8:00 am and 9:30 pm, EST, Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Art Unit: 2186

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

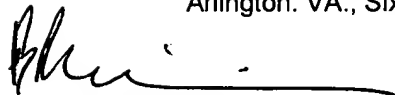
or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,
Arlington, VA., Sixth Floor (Receptionist).



B. James Peikari
Primary Examiner
Art Unit 2186

4/5/04